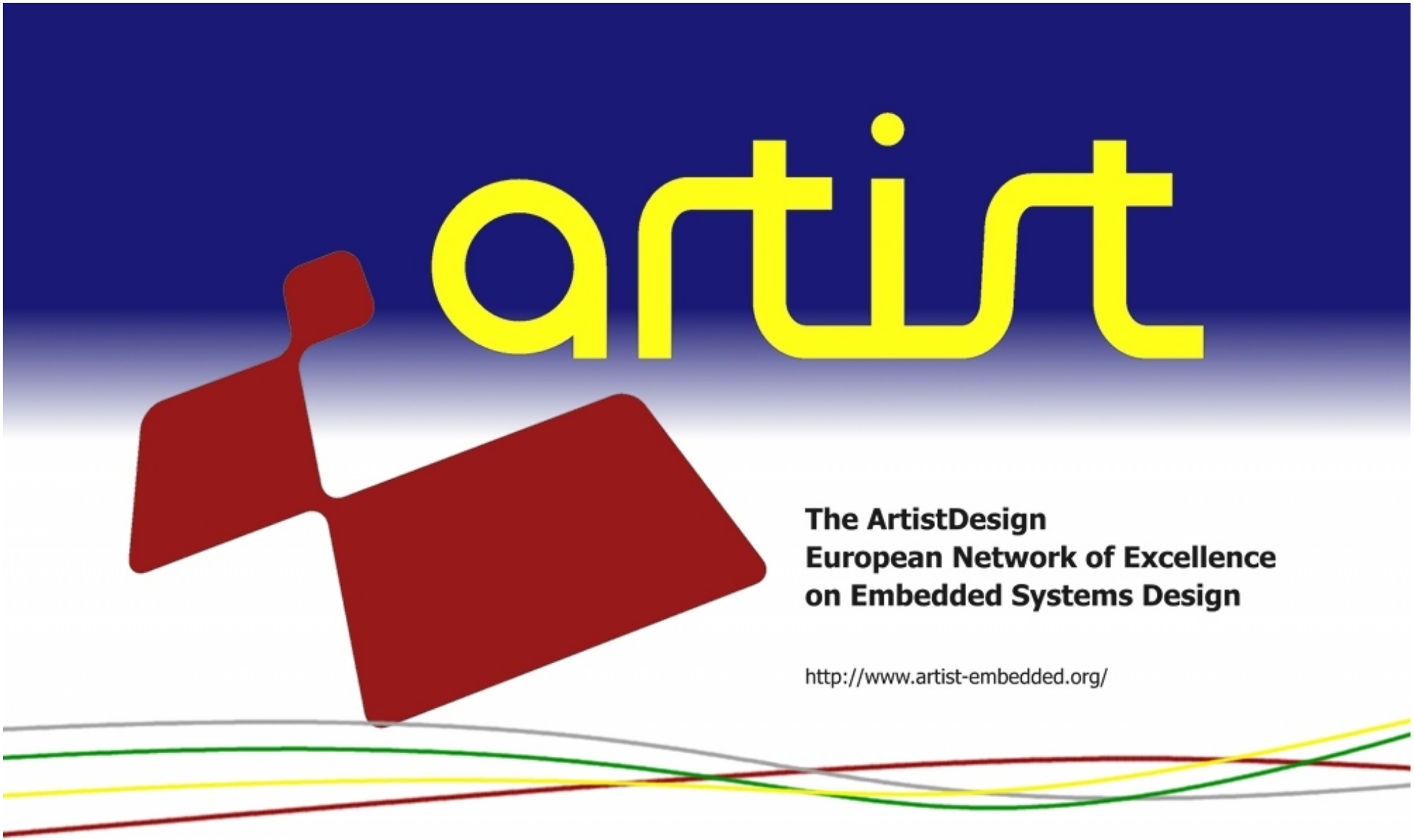


Showcase of the Main Results

DATE Conference, March 15th, 2012

SEVENTH FRAMEWORK PROGRAMME

ArtistDesign European NoE: Showcase of the Main Results

DATE Conference, March 15th, 2012

Achievements and Perspectives :

ArtistDesign Network of Excellence

scientific coordinator: Joseph Sifakis

technical coordinator: Bruno Bouyssounouse

Concepts and Objectives – Main Ideas

Main Idea 1

- *Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services.*
  This is well-recognized in the ICT FP7 priorities, and through the ARTEMIS ETP.

Main Idea 2

- *Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems.*
- *For this discipline to emerge, a considerable focused research effort by the best teams is needed.*

Objectives

Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

- The NoE acts as a Virtual Center of Excellence
- **Two levels** of integration
  to create critical mass from selected European teams
  - **Strong integration** within selected topics
    by assembling the best European teams,
    to advance the state of the art in the topic.
  - Integration **between** topics
    to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.
- Integration is around a Joint Programme of Activities

Core Participants (1/2)

N°	Beneficiary name	Beneficiary short name	Country
1	UJF FILIALE	FLORALIS	France
2	UNIVERSITE JOSEPH FOURIER GRENOBLE 1	UJF/VERIMAG	France
3	AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INRIA	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden

Core Participants (2/2)

N°	Beneficiary name	Beneficiary short name	Country
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
24	UNIVERSITAET PASSAU	PASSAU	Germany
25	SCUOLA SUPERIORE DI STUDI UNIVERSITARI E DI PERFEZIONAMENTO SANT'ANNA	SSSA-PISA	Italy
26	INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO	PORTO	Portugal
27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK
32	IST-AUSTRIA	IST-Austria	Austria
33	UNIVERSITY OF PORTO	UnivPorto	Portugal
34	UNIVERSITY OF TRENTO	TRENTO	Italy

Theory, Methods and Tools for ES Design

Design flow involves topics leading from initial requirements to a final implementation satisfying them. The objective is to study specific needs for these design activities, as well the possibility of integrating them in a coherent design flow.

We distinguish four essential topics, for which existing techniques should be adapted and extended :

- **Modelling and Validation**: We need formal modelling techniques that take into account the characteristics of a system's external and execution environments. These techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.
- **Software Synthesis, Code Generation and Timing Analysis**: Strong integration should be sought for these interrelated topics. The aim is to study and implement resource-aware synthesis and code generation techniques. These techniques allow the generation of an implementation meeting given user requirements from a functional description of an application (e.g. application software) and a model of a target platform.
- **Real-Time Operating Systems Scheduling and Networks**: The aim is to develop theory methods and tools for new real-time software infrastructures, for the execution and communication between embedded applications. The main problems include adaptive resource management and dependability techniques, in particular to improve robustness to deviations from nominal conditions.
- **Platforms and MPSoC Design**: The aim is implementation of complex applications on multi-core HW platforms. It raises a number of problems for ensuring predictability and efficiency. These include adaptive techniques for resource management, and the study of reliable programming models for multi-core architectures.

Long Term Integration

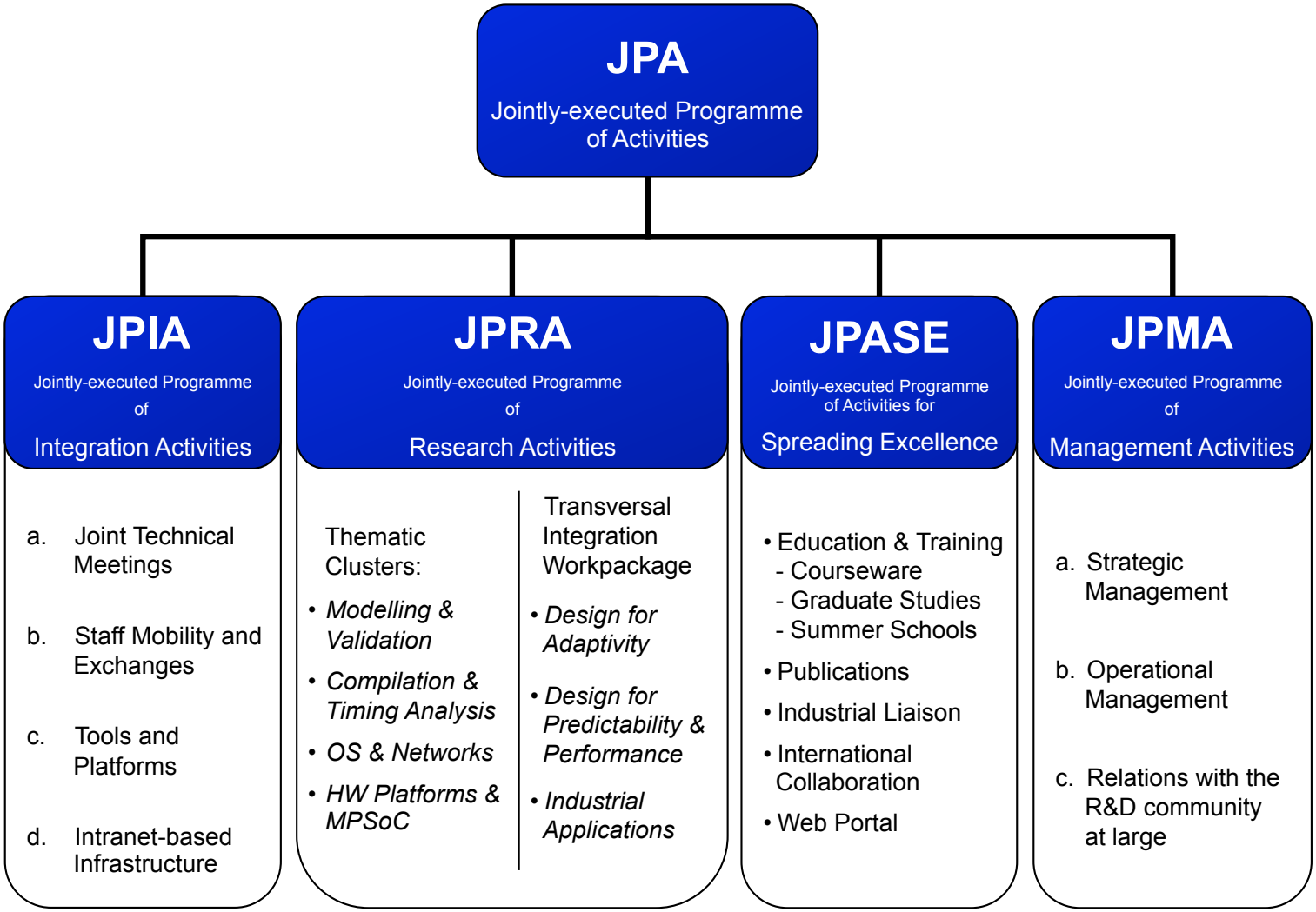
Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas.

ArtistDesign continues and extends these activities, both quantitatively and qualitatively. In setting up the consortium, we have the right balance between critical mass, excellence, and commitment from the core partners.

- **Critical Mass**
  We have a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as the capacity to impact the European research landscape. Nonetheless, to ensure efficiency, we have limited the number of core partners, based on previous experience. At the same time, our impact is amplified through the large number of affiliated academic, SME, industrial, and international collaboration partners.
- **Excellence**
  The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.
- **Commitment**
  The majority of the ArtistDesign core partners were already involved as core partners in the Artist2 NoE. They have demonstrated a high degree of investment to achieve the workprogramme objectives, by committing the resources needed, which are an order of magnitude larger than those provided by the NoE financing. We estimate that the effort for implementing the JPA is roughly 10 times the financial contribution for integration.

Joint Programme of Activities

ArtistDesign acts as a Virtual Centre of Excellence, composed of a set of virtual teams, called clusters. Each cluster gathers together selected teams from partners, to create the critical mass and expertise in one of the essential topics for embedded systems design.



Jointly-executed Programme of Integrating Activities (JPIA)

- Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. Funds for staff mobility are allocated by taking into account the needs for research.

  - **Joint Technical Meetings**
    Present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

  - **Staff Mobility and Exchanges**
    Mobility is justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

  - **Tools and Platforms**
    Research platforms lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. Some of these have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

Joint Programme of Activities for Spreading Excellence (JPASE)

These NoE-level activities serve as a relay between the NoE and the international embedded systems design community at large.

- **Education and Training**
  These actions serve as incubators for developing integrated curricula and materials, and to disseminate results and spread excellence well beyond the partners and affiliated partners of ArtistDesign.

- **Publications in Conferences and Journals**
  Implemented through publication in the main conferences on Embedded Systems Design of the area, as well as the active participation for the organization and management of these events.

- **Industrial Liaison**
  This consists of actions oriented towards affiliated industrial partners, to transfer results follow and get feedback on the research and integration activities in the JPA (JPRA, JPIA).

- **International Collaboration**
  These activities play a dual role: showcase the participants' results, and reinforce the NoE's leadership role worldwide. They will also collect relevant information about evolution of the state of the art outside Europe.

- **Web Portal**
  This plays a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large, and be an essential mechanism for achieving integration and recognition.

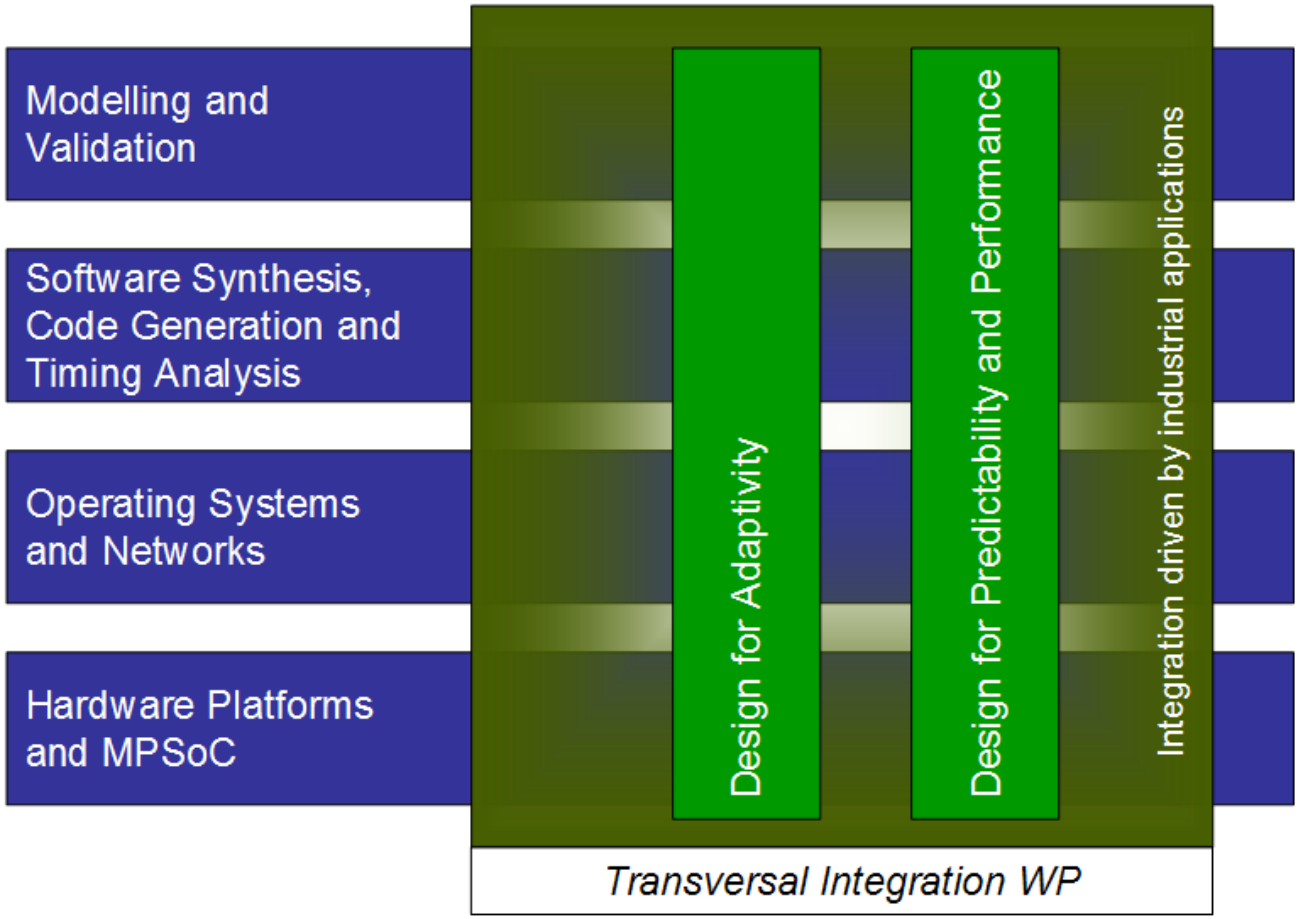
Summary of the ArtistDesign Research Activities

Jointly-executed Programme of Research Activities (JPRA)

Clusters are autonomous entities, with specific objectives, teams, leaders, and a dedicated yearly budget.

The set of Thematic Clusters cover all the main topics in Embedded Systems Design. The thematic activities in the Transversal Integration workpackage focus on Design methodologies, with specific objectives (Predictability, Adaptivity).

Each cluster may have one or several Activities, as appropriate.



Thematic Cluster: Modeling and Validation

cluster leaders: Kim Larsen (Aalborg) + Susanne Graf (Verimag)

JPRA Activity: "Modeling"

Suzanne Graf (Verimag - France)

Develop model- and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. Simultaneously address software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based.

JPRA Activity: "Validation"

Kim Larsen (Aalborg - Denmark)

Designing scalable techniques allowing for efficient and accurate analysis of performance and dependability issues with respect to the various types of (quantitative) models considered, covering a range of model-based validation techniques ranging from simulation, testing, model-checking, compositional techniques, refinement and abstract interpretation.

Thematic Cluster:

Software Synthesis, Code Generation and Timing Analysis

cluster leader:
Peter Marwedel (Dortmund)

JPRA Activity: "Software Synthesis, Code Generation "

Peter Marwedel (Dortmund - Germany)

Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. It can also be expected that the link between software engineering and embedded systems will become stronger.

JPRA Activity: "Timing Analysis"

Björn Lisper (Mälardalen - Sweden)

Timing analysis of MPSoC systems is a new scientific field, and is very timely from an application perspective as MPSoC and Multicore architectures rapidly are becoming mainstream. A research effort in this area will thus establish European dominance in a field that rapidly is becoming very important.

Thematic Cluster: Operating Systems and Networks

cluster leader:
Giorgio Buttazzo (Pisa - Italy)

JPRA Activity: "Resource-Aware Operating Systems" *Giorgio Buttazzo (Pisa - Italy)*

Investigate how RTOS have to be extended or modified to support emerging RT embedded systems (high complexity, highly variable resource requirements and parallel processing). Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, while guaranteeing isolation properties.

JPRA Activity: "Scheduling and Resource Management" *Alan Burns (York - UK)*

Provision of models of embedded platform resources and policies, and the necessary analysis for undertaking the run-time scheduling of these resources and policies. A key scientific challenge is to link this resource-centred analysis with models of the application (and their resource usage policies) and the performance profiles of the hardware platform itself.

JPRA Activity: "Real-Time Networks" *Luis Almeida (U. Aveiro – Portugal)*

This activity addresses numerous research challenges in the frameworks of Networked Embedded Systems (NESs), Wireless Sensor Networks (WSNs) and Mobile Ad-hoc Networks (MANETs).

Thematic Cluster: # Hardware Platforms and MPSoC

cluster leader:
Jan Madsen (DTU - Denmark)

JPRA Activity: "Platform and MPSoC Design"

Luca Benini (U. Bologna - Italy)

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, runt-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations.

JPRA Activity: "Platform and MPSoC Analysis"

Jan Madsen (DTU - Denmark)

Establish a set of models and analysis methods that scales to massively parallel and heterogeneous multiprocessor architectures, is applicable to distributed embedded systems as well, allows for the analysis of global predictability and efficiency system properties and takes the available hardware resources and the corresponding sharing strategies into account.

Transversal Integration

WP leader:
Alberto Sangiovanni (Trento - Italy)

JPRA Activity: "Design for Adaptivity"

Karl-Erik Årzén (Lund University – Sweden)

An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is required both off-line at design-time and on-line at run-time. Off-line adaptivity is required to handle changing system specifications and to support platform-based or product-family based development.

JPRA Activity: "Design for Predictability and Performance"

Bengt Jonsson (Uppsala - Sweden)

The technical achievements contribute to a suite of techniques across the abstraction levels of embedded system design, including application modelling and analysis, scheduling support, compilers, and platform design techniques. The achievements will also entail interfacing of existing tools for design of embedded systems.

JPRA Activity: "Integration Driven by Industrial Applications"

Alberto Sangiovanni (Trento – Italy)

The ultimate goal of this activity is to provide the "meta rules" according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable.

Summary of the ArtistDesign Results

Cluster: Modeling and Validation

Interaction and Research activities have progressed substantially :

Modelling:

- Composition frameworks for behaviour and properties of heterogeneous systems such as assume/guarantee reasoning, interface automata, modal transition systems as well as composition frameworks for tool integration based on meta-models and model-transformations have been consolidated and applied to case studies.
- Resource modelling techniques applied to design space exploration, multi-core scheduling, performance evaluation and derivation of distributed implementations from global specifications.
- Quantitative modelling techniques for weighted automata, priced timed automata and quantitative communication models.

Validation:

- Quantitative Validation covering a wide range of techniques for WCET analysis, schedulability analysis, frequency analysis of timed automata, analysis of parametric quantitative models, and analysis of resource consumption using energy- and price-extensions of timed automata. These techniques use new notions of metrics and robustness.
- Cross-Layer Validation focusing on model-based testing techniques such conformance testing of real-time systems using time- and data abstractions, asynchronous testing and test-case generation for embedded Simulink, incremental testing of composite systems as well as runtime monitoring.
- Compositional validation

Also, the Cluster has endeavoured a considerable integration effort for connecting tools, joint meetings, open workshops and joint publications.

Cluster: SW Synthesis, Code Gen and TA

- Global activities: Leading-edge educational material in 2nd edition of the textbook on embedded systems, work on predictability, industrial applications
- Importance of multi-processor systems growing. ArtistDesign is active in this area.
- Work on code generation focused on tools for mapping applications to multi-cores (RWTH Aachen, IMEC, Dortmund, affiliates).
- Work on resource-aware compilation: New results on energy efficiency & thermal behavior, fundamental machine-learning techniques for optimized code generation.
- Software Synthesis: Series of workshops + contributions to *Industrial Informatics*
- In program flow analysis, MDH and Tidorum: advanced relational value analysis that takes possible overflows and wraparounds into account.
- Work on timing analysis and timing predictability progressed:
  - Enforcing predictability through determinism. Industrially relevant results on cache analysis & cache-aware memory allocation, *used in commercial tools.*
  - Randomization to make timings on micro-level independent: *very promising*.
- Advances in hybrid WCET analysis methods, including measurements and testing (MDH, York, TU Vienna).
- Integration of timing analysis tools and compilation tools (TU Dortmund, TU Vienna).

Cluster: Operating Systems and Networks

The work in the cluster involved several partners that produced significant results summarized as follows:

- The work on operating systems and middleware focuses on resource reservation and predictability.
  - Implementation of a real-time scheduler in the Linux kernel, with support for resource reservation.
  - Developed a programming framework to support resource reservation of concurrent real-time applications on multi-core platforms, considered by Ericsson for software development in next generation cell phones.
  - Proposed a comprehensive taxonomy for the resources currently used in embedded real-time systems.
- Work on predictability includes cache-aware analysis and scheduling for safety-critical applications, In collaboration with the Cluster on Compilers and Timing analysis.
- The cluster also developed a middleware and communication protocol for teams of mobile robots that are self-reconfigurable and provide efficient support to intensive interactions and which have been adopted by several teams in the RoboCup Middle Size League.
- The work on networks includes two toolsets. One for the design, analysis, configuration and deployment of dense WSNs. The other is the MAST (Modelling and Analysis Suite for Real-Time Applications), which was enhanced with more networking components and analysis, namely for switched networks such as AFDX. Also a number of communication protocols and tools, developed for improving predictability and adaptivity in (industrial) networked embedded systems.

Finally, the cluster teams have been involved in many European projects, had strong interaction with industry and disseminated their work through active participation in world class conferences, workshops and schools.

Cluster: HW Platform and MPSoC Design (1/2)

The Cluster has continued its efforts to establish an integrated modelling and design methodology that can take into account predictability and resource-awareness with focus on efficiency. This work has benefited from fruitful collaboration with the Cluster on Modelling and Validation and Timing Analysis as well as from the transversal activities on design from adaptivity and predictability.

Main results can be summarized as follows:

- Fault tolerant distributed embedded systems: We have developed results for handling both processor and communication faults in distributed real-time systems for automotive applications, based on CAN or FlexRay communication.
- Performance analysis methods: TU Braunschweig and ETH Zurich have developed very original and relevant results. They have collaborated to establish a method for coupling the tools SymTA/S and MPA. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.
- MPSoC design: Major activities on MPSoC design have focused on application parallelization, platform mapping, memory hierarchy management, application scenario exploitation, and run-time resource management, including reconfigurable systems. The outcome of these 4 years was the development of related tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.

Cluster: HW Platform and MPSoC Design (2/2)

- Energy harvesting: We have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU), and have demonstrated that these techniques can lead to considerable extensions of the lifetime of the network. One specific outcome is the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) that aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities.
- Temperature and energy aware optimization: EPFL has developed a novel online thermal management policy based on dynamic voltage and frequency scaling for high-performance 3-D systems with liquid cooling. The approach is able to gain up to 50% as compared to current state-of-the-art thermal control techniques.

Finally, the Cluster has an impressive record of joint publications, invited talks, analysis and design tools and industrial collaborations.

Transversal Integration: Design for Adaptivity

(1/3)

The work done includes numerous highlights:

- Scheduling analysis:
  - Efficient and effective scheduling analysis for fixed priority systems has been developed that takes into account tasks arriving and leaving the system.
  - A new method for allocation and scheduling of parallel tasks in soft-real time systems (multimedia decoding) in the presence of post-silicon, process and ageing induced variability in a nominally homogeneous target multi-core platform has been developed.
- Memory: Dynamically adaptable memory architectures for supporting dynamic real-time process loads have been developed.
- Collaboration frameworks: An adaptable cooperation-based framework for networked embedded systems with heterogeneous nodes has been developed, allowing constrained devices to cooperate with more powerful (or less congested) neighbours, to meet allocation requests and handle stringent constraints, opportunistically taking advantage of global resources and processing power.
- Service adaptation: Techniques have been developed for adapting the service request handling behaviour to the specific requirements of the services in Service Oriented Architectures (SOA). CPU contracts are used to ensure sufficient computation time for dealing with services with special requirements.

Transversal Integration: Design for Adaptivity

(2/3)

- Run-time resource management: An adaptive resource manager for distributed embedded systems aimed at multimedia applications, e.g., broadcast management systems, was developed. Considerable savings in power consumption, hardware cost and system size were reported in an industrial case study. Parallel to this a QoS based adaptive resource management system for homogeneous multicore platforms was developed.

- Run-time analysis: A distributed approach for in-system run-time performance analysis of embedded systems, complemented by a framework enabling access control and runtime-optimization through the use of distributed algorithms.

- Sensor networks: New approaches to adaptive energy management of energy harvesting system using solar cells have been developed. Based on a prediction of the future available energy, the application parameters are adapted in order to maximize the utility in a long-term perspective.

- Control techniques: A new method for optimizing the timing parameters of real-time control tasks in resource-constrained embedded systems has been derived. Also, new feedback scheduling techniques and new event-driven sampling mechanisms have been proposed.

- Adaptivity in networks: Here various ways of adapting a communication channel to varying application requirements or environmental conditions to enhance the efficiency of medium utilization have been proposed. For controlled access networks with isolated virtual channels the guaranteed bandwidth and latency can be adapted online using the Flexible Time-Triggered (FTT) paradigm on switched Ethernet, either with COTS switches (FTT-SE protocol) or enhanced ones (FTT-enabled switch).

Transversal Integration: Design for Adaptivity

- Programmable hardware: A new type of ultra-fault-tolerant FPGA named the eDNA architecture has been conceived all the way from development of the concept, to the implementation of a prototype, to test in a space related case study NASA JPL.

- WCET analysis: Parametric WCET bounds, where the WCET bound depends on the values of certain inputs, can be used in adaptive real-time systems where the scheduling of tasks adapts to external factors such as varying data sizes affecting the running times of tasks. A general method for parametric WCET analysis, which combines a number of advanced symbolic techniques including relational abstract interpretation, counting of integer points in polyhedra, and parametric integer programming has been developed and implemented in the WCET analysis tool SWEET.

- Reference architectures: A reference architecture for automotive embedded systems that addresses the needs for flexible and automatic run-time reconfiguration has been proposed. The research focus was the development of technical support in terms of middleware services for a closed adaptation of distributed embedded systems. In addition to the reference architecture an information model of the control parameters that represent the target system configuration alternatives, environmental parameters, and internal conditions has been defined and a functional design has been performed.

Insights gained for Adaptivity

1. The increasing complexity, the hardware development, the demands for resource efficiency, and the increasing reliance on software and/or programmable approaches in embedded systems will without doubt increase the demands for adaptivity in the future.

2. Adaptivity in embedded systems covers a wide range of subjects. Hence, to develop a common theoretical basis for adaptivity in embedded systems is extremely challenging. The work performed within ArtistDesign can merely be considered as a starting point for this.

3. In order to move adaptivity from the research community to industrial practice it is essential that adequate support for adaptivity is included in COTS software and hardware, including OS and middleware. This include sensing and actuation mechanisms, models (thermal, battery, power, …) with correct parameters, and an adaptivity API between applications and OS/middleware.

4. There is a fundamental tradeoff between adaptivity and predictability. Hence, for applications with severe requirements on predictability, adaptive mechanisms are less suitable. Furthermore, adaptivity makes formal verification more difficult So maybe adaptivity is not suitable for hard RT, time-critical systems? However, as soon as fault tolerance and reconfigurability becomes design requirements we need adaptivity.

5. The adaptation mechanisms must be very resource efficient and the requirements which they pose on the applications and the knowledge they require about the applications must be small. Therefore adaptation mechanisms must be quite simple in order to be practically useful.

6. The thermal control, power control, and performance control needed in multi/many-core embedded systems have very strong relationships with the same problems in data centers. Hence, a unified approach to resource management of computing systems is a realistic future goal.

Transversal Integration: (1/2)

Design for Predictability and Performance

Intersection with all the thematic clusters, eg:

- The Predator project has made strong progress in its attempt to reconcile Predictability with Performance.
  - Integration of the AbsInt timing-analysis tool aiT with the WCET-aware compiler of TUDortmund
  - determination of context-switch costs, schedulability analysis for preemptive scheduling strategies.
  - Insights into the predictability properties of architectural features have found their way into the embedded-systems industry, e.g., as a result of collaboration in European projects.

- Trends to multi-core platforms present a significant challenge to the building of predictable and performant systems, and there is still significant hesitation to migrating embedded systems to multi-cores. Significant advances on isolation and analysis techniques have been made (to a large extent by ARTIST-Design partners): progress is made, e.g., in the area of deterministic access protocols and controllers for shared resources such as buses or memory. However, the worst-case delay used in safe approximations is still often too high to be acceptable.

- A good collection of insights was gathered at the PPES workshop, organized by ARTIST-Design, jointly with Predator and Merasa, as a satellite event of DATE 2011 in Grenoble. Overviews about architecture and software issues were given, e.,g including a survey on predictability and performance requirements in avionics systems, and a template for, partly analytically, partly intuitively, estimating the predictability of hardware features was presented.

Transversal Integration: (2/2)

Design for Predictability and Performance

- During year 4, development of support for the MARTE standard (initiated during ARTIST2), led by U. Cantabria, has provided increased support for scheduling and code generation. The work on integration between timing analysis tools has matured: several of the leading timing analysis tools have been integrated by efforts in the All-Times project (described in the report on Timing analysis).

- A notable trend during Year 4 has been the work on reconciling predictability with performance, developing techniques for optimizing performance along several dimensions (e.g., combing WCET with average-case timing). Work in this direction (by Bologna, ETHZ, Linköping, Trento) has considered different forms of multi-objective optimization of embedded software; such possibilities also exist in the WCC compiler. Another increasingly important topic has been to make scheduling and timing analysis robust to inaccuracies in assumptions about, e.g., execution times, interferences, etc.

- Work on the integration of timing analysis and compilation, in the context of the WCC compiler, aimed at removing some of the earlier restrictions. The work started at TU Dortmund considering WCET-aware basic block reordering has been finished.

Transversal Integration:

Industrial Integration

- This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.
- The activities include both technical achievements and dissemination work on the following: General Frameworks for system-level design; Applications to the Automotive Sector; Applications to Chip Design; Applications to Buildings; Applications to Wireless communication technology; Timing Analysis and Predictability; Other Applications.
- Industrial interactions and collaborations with ArtistDesign teams is substantial with the participation of Partners in more than 10 Artemis Projects and with the participation of the industrial activities in start-ups (more than 8).
- The level of energy at the meetings organized to foster industrial integration was excellent. This theme is of increased interest to the European community in response to energy conservation concerns.

Spreading Excellence in Y4

ARTIST Summer School in Europe 2011 - 7th edition

- high quality technical programme, excellent feedback from participants
- 73 paying participants and 14 invited speakers.

International ARTIST Summer School in China 2011 – 6th edition

Graduate Schools:

- **ARTIST Quantitative Model Checking Winter School 2012**
  February 27th - March 1st 2012 Copenhagen, Denmark
- **Time-Predictable and Composable Architectures for Dependable Embedded Systems**
  October 9th, 2011 Taipei, Taiwan
- **ARTIST Summer School on ICT for Future Energy Systems**
  July 25-29, 2011 Povo, Trento, Italy
- **ARTIST Graduate School on RT Kernels for Microcontrollers**
  June 13-17, 2011 Pisa, Italy

ARTIST Workshops

NERES, ACES^{MB}, WSS'11, WESE, TP&CADES, JTRES, FORMATS, IRTAW-15, WCET, RTN, Map2MPSoC, APRES, RED, PPES, ArtistDesign Workshop on Real-Time System Models for Schedulability Analysis, Synchronous Programming of Device Drivers for Global Resource Control in Embedded Operating Systems

ARTIST web portal

Summary of Achievements

Artist has clearly met and well exceeded its goals. Artist has achieved a level of real integration between leading teams that would have been unimaginable before the NoE. The level of integration and excellence achieved through Artist are well beyond the funding allocated.

Integration and excellence can be measured by:

- Number of joint publications
- Number and quality of collaborative submitted and funded projects
- Number of dissemination events including workshops, graduate schools, and international summer schools
- A common vision for structuring the effort in the area

Unprecedented level of interaction with industry as attested by

- Participation of industrial partners in the projects and technical meetings
- Active participation in setting up Artemis and Artemisia
- Transfer of methods and tools

International recognition as attested by

- collaborations with leading research teams in the US and Asia
- active involvement of Artist teams in steering main flagship events in the area

THANK YOU